V1720
Registers
Description

22 April 2013

MOD. V1720
8 CHANNEL 12 BIT
250 MS/S DIGITIZER

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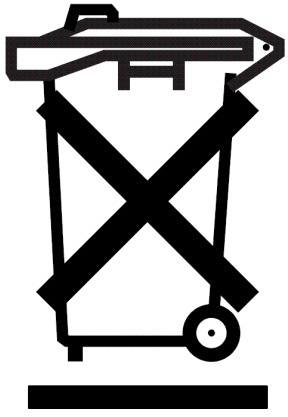

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1. Important Notices

The content of this document has been extracted from:

V1720 & VX1720 User Manual – Revision N. 21 – Date: 06 February, 2012

FOR RELEASES OF THE ROC FPGA FIRMWARE HIGHER THAN 3.8 THE CONTENT OF THIS DOCUMENT MAY RESULT NOT FULLY COMPLIANT.

IT IS INTENDED TO BE REPLACED BY A NEW DOCUMENT UNIFYING THE REGISTERS DESCRIPTIONS OF CAEN DIGITIZERS CURRENTLY IN PROGRESS.

2. VME Interface

The following sections will describe in detail the VME-accessible registers content.

⚠ N.B.: bit fields that are not described in the register bit map are reserved and must not be over written by the User.

2.1. Registers address map

Table 2.1: Address Map for the Model V1720

REGISTER NAME	ADDRESS	ASIZE	DSIZE	MODE	H_RES	S_RES	CLR
EVENT READOUT BUFFER	0x0000-0x0FFC	A24/A32/A64	D32	R	X	X	X
Channel n ZS_THRES	0x1n24	A24/A32	D32	R/W	X	X	
Channel n ZS_NSAMP	0x1n28	A24/A32	D32	R/W	X	X	
Channel n THRESHOLD	0x1n80	A24/A32	D32	R/W	X	X	
Channel n TIME OVER/UNDER THRESHOLD	0x1n84	A24/A32	D32	R/W	X	X	
Channel n STATUS	0x1n88	A24/A32	D32	R	X	X	
Channel n AMC FPGA FIRMWARE REVISION	0x1n8C	A24/A32	D32	R			
Channel n BUFFER OCCUPANCY	0x1n94	A24/A32	D32	R	X	X	X
Channel n DAC	0x1n98	A24/A32	D32	R/W	X	X	
Channel n ADC CONFIGURATION	0x1n9C	A24/A32	D32	R/W	X	X	
CHANNEL CONFIGURATION	0x8000	A24/A32	D32	R/W	X	X	
CHANNEL CONFIGURATION BIT SET	0x8004	A24/A32	D32	W	X	X	
CHANNEL CONFIGURATION BIT CLEAR	0x8008	A24/A32	D32	W	X	X	
BUFFER ORGANIZATION	0x800C	A24/A32	D32	R/W	X	X	
BUFFER FREE	0x8010	A24/A32	D32	R/W			
CUSTOM SIZE	0x8020	A24/A32	D32	R/W	X	X	
ACQUISITION CONTROL	0x8100	A24/A32	D32	R/W	X	X	
ACQUISITION STATUS	0x8104	A24/A32	D32	R			
SW TRIGGER	0x8108	A24/A32	D32	W			
TRIGGER SOURCE ENABLE MASK	0x810C	A24/A32	D32	R/W	X	X	
FRONT PANEL TRIGGER OUT ENABLE MASK	0x8110	A24/A32	D32	R/W	X	X	
POST TRIGGER SETTING	0x8114	A24/A32	D32	R/W	X	X	
FRONT PANEL I/O DATA	0x8118	A24/A32	D32	R/W	X	X	
FRONT PANEL I/O CONTROL	0x811C	A24/A32	D32	R/W	X	X	
CHANNEL ENABLE MASK	0x8120	A24/A32	D32	R/W	X	X	
ROC FPGA FIRMWARE REVISION	0x8124	A24/A32	D32	R			
EVENT STORED	0x812C	A24/A32	D32	R	X	X	X
SET MONITOR DAC	0x8138	A24/A32	D32	R/W	X	X	

REGISTER NAME	ADDRESS	ASIZE	DSIZE	MODE	H_RES	S_RES	CLR
BOARD INFO	0x8140	A24/A32	D32	R			
MONITOR MODE	0x8144	A24/A32	D32	R/W	X	X	
EVENT SIZE	0x814C	A24/A32	D32	R	X	X	X
VME CONTROL	0xEF00	A24/A32	D32	R/W	X		
VME STATUS	0xEF04	A24/A32	D32	R			
BOARD ID	0xEF08	A24/A32	D32	R/W	X	X	
MULTICAST BASE ADDRESS & CONTROL	0xEF0C	A24/A32	D32	R/W	X		
RELOCATION ADDRESS	0xEF10	A24/A32	D32	R/W	X		
INTERRUPT STATUS ID	0xEF14	A24/A32	D32	R/W	X		
INTERRUPT EVENT NUMBER	0xEF18	A24/A32	D32	R/W	X	X	
BLT EVENT NUMBER	0xEF1C	A24/A32	D32	R/W	X	X	
SCRATCH	0xEF20	A24/A32	D32	R/W	X	X	
SW RESET	0xEF24	A24/A32	D32	W			
SW CLEAR	0xEF28	A24/A32	D32	W			
FLASH ENABLE	0xEF2C	A24/A32	D32	R/W	X		
FLASH DATA	0xEF30	A24/A32	D32	R/W	X		
CONFIGURATION RELOAD	0xEF34	A24/A32	D32	W			
CONFIGURATION ROM	0xF000-0xF3FC	A24/A32	D32	R			

2.2. Configuration ROM (0xF000-0xF084; r)

The following registers contain some module's information, they are D32 accessible (read only):

- **OUI**: manufacturer identifier (IEEE OUI)
- **Version**: purchased version
- **Board ID**: Board identifier
- **Revision**: hardware revision identifier
- **Serial MSB**: serial number (MSB)
- **Serial LSB**: serial number (LSB)

Table 2.2: ROM Address Map for the Model V1720

Description	Address	Content
checksum	0xF000	*0xA4*
checksum_length2	0xF004	0x00
checksum_length1	0xF008	0x00
checksum_length0	0xF00C	0x20
constant2	0xF010	0x83
constant1	0xF014	0x84
constant0	0xF018	0x01
c_code	0xF01C	0x43
r_code	0xF020	0x52
oui2	0xF024	0x00
oui1	0xF028	0x40
oui0	0xF02C	0xE6
vers	0xF030	V1720, VX1720: 0x30 V1720B, VX1720B: 0x31 V1720C, VX1720C: 0x32 V1720D, VX1720D: 0x33 V1720E, VX1720E: 0x35 V1720F, VX1720F: 0x36 V1720G: 0x37
board2	0xF034	V1720: 0x00 VX1720: 0x01
board1	0xF038	0x06
board0	0xF03C	0xB8
revis3	0xF040	*0x00*
revis2	0xF044	*0x00*
revis1	0xF048	*0x00*
revis0	0xF04C	*0x01*
sernum1	0xF080	*0x00*
sernum0	0xF084	*0x16*

These data are written into one Flash page; at Power ON the Flash content is loaded into the Configuration RAM, where it is available for readout.

2.3. Channel n ZS_THRES (0x1n24; r/w)

Bit	Function
[31]	0 = Positive Logic 1 = Negative Logic
[30:11]	*reserved*
[11:0]	With “Full Suppression based on the amplitude”, the 12 LSB represent the value to be compared with each sample of the event; and see if it is over/unedr threshold (depending on the used logic). With “Zero Length Encoding”, the 12 LSB represent the value to be compared with each sample of the event, and see if it is “good” or “skip” type).

2.4. Channel n ZS_NSAMP (0x1n28; r/w)

Bit	Function
[31:0]	With “Full Suppression based on the amplitude” (ZS AMP), bits [20:0] allow to set the number Ns of subsequent data which must be found over/under threshold (depending on the used logic) necessary to validate the event; if this field is set to 0, it is considered “1”. With “Zero length encoding” (ZLE) bit [31:16] allows to set/read N_{LBK}: the number of data to be stored before the signal crosses the threshold. bit [15:0] allows to set/read N_{LFWD}: the number of data to be stored after the signal crosses the threshold)

2.5. Channel n Threshold (0x1n80; r/w)

Bit	Function
[11:0]	Threshold Value for Trigger Generation

Each channel can generate a local trigger as the digitised signal exceeds the Vth threshold, and remains under or over threshold for Nth [4 samples; 5 samples in Pack2.5 mode] at least; local trigger is delayed of Nth [4/5 samples] with respect to input signal. This register allows to set Vth (LSB=input range/12bit).

2.6. Channel n Over/Under Threshold (0x1n84; r/w)

Bit	Function
[11:0]	Number of Data under/over Threshold

Each channel can generate a local trigger as the digitised signal exceeds the Vth threshold, and remains under or over threshold for Nth [4/5 samples] at least; local trigger is delayed of Nth [4 samples; 5 samples in Pack2.5 mode] with respect to input signal. This register allows to set Nth.

2.7. Channel n Status (0x1n88; r)

Bit	Function
[5]	Buffer free error: 1 = trying to free a number of buffers too large
[4:3]	*reserved*
[2]	Channel n DAC (see § 2.10) Busy 1 = Busy 0 = DC offset updated
[1]	Memory empty
[0]	Memory full

2.8. Channel n AMC FPGA Firmware (0x1n8C; r)

Bit	Function
[31:16]	Revision date in Y/M/DD format
[15:8]	Firmware Revision (X)
[7:0]	Firmware Revision (Y)

Bits [31:16] contain the Revision date in Y/M/DD format.
Bits [15:0] contain the firmware revision number coded on 16 bit (X.Y format).
Example: revision 1.3 of 12th June 2007 is: 0x760C0103

2.9. Channel n Buffer Occupancy (0x1n94; r)

Bit	Function
[10:0]	Occupied buffers (0..1024)

2.10. Channel n DAC (0x1n98; r/w)

Bit	Function
[15:0]	DAC Data

Bits [15:0] allow to define a DC offset to be added the input signal in the ±1V range. When Channel n Status bit 2 is set to 0, DC offset is updated (see § 2.7).

2.11. Channel n ADC Configuration (0x1n9C; r/w)

Bit	Function
[15:0]	T.B.D.

This register allows to pilot the relevant ADC signals. See the LTC2242-12 - 12-Bit, 250Msps ADC data sheet for details.

2.12. Channel Configuration (0x8000; r/w)

Bit	Function
[19:16]	Allows to select Zero Suppression algorithm: 0000 = no zero suppression (default); 0010 = zero length encoding (ZLE); 0011 = full suppression based on the amplitude (ZS AMP)
[18:12]	*reserved*
[11]	0 = Pack2.5 disabled 1 = Pack2.5 enabled
[10:7]	*reserved*
[6]	0 = Trigger Output on Input Over Threshold 1 = Trigger Output on Input Under Threshold allows to generate local trigger either on channel over or under threshold (see § 2.3 and § 2.6)
[4]	0 = Memory Random Access 1 = Memory Sequential Access
[3]	0 = Test Pattern Generation Disabled 1 = Test Pattern Generation Enabled
[1]	0 = Trigger Overlapping Not Enabled 1 = Trigger Overlapping Enabled Allows to handle trigger overlap
[0]	*reserved*

This register allows to perform settings which apply to all channels.
It is possible to perform selective set/clear of the Channel Configuration register bits writing to 1 the corresponding set and clear bit at address 0x8004 (set) or 0x8008 (clear) see the following § 2.13 and 2.14. Default value is 0x10.

2.13. Channel Configuration Bit Set (0x8004; w)

Bit	Function
[7:0]	Bits set to 1 means that the corresponding bits in the Channel Configuration register are set to 1.

2.14. Channel Configuration Bit Clear (0x8008; w)

Bit	Function
[7:0]	Bits set to 1 means that the corresponding bits in the Channel Configuration register are set to 0.

2.15. Buffer Organization (0x800C; r/w)

Bit	Function
[3:0]	BUFFER CODE

The BUFFER CODE allows to divide the available Output Buffer Memory into a certain number of blocks, according to the following table:

Table 2.3: Output Buffer Memory block division

REGISTER	BUFFER NUMBER	SIZE of one BUFFER (samples)			
		SRAM 1.25MS/ch (V1720/C/E/F)		SRAM 10MS/ch (V1720B/D/G)	
		Std.	Pack2.5	Std.	Pack2.5
0x00	1	1M	1.25M	8M	10M
0x01	2	512K	640K	4M	5M
0x02	4	256K	320K	2M	2.5M
0x03	8	128K	160K	1M	1.25M
0x04	16	64K	80K	512K	640K
0x05	32	32K	40K	256K	320K
0x06	64	16K	20K	128K	160K
0x07	128	8K	10K	64K	80K
0x08	256	4K	5K	32K	40K
0x09	512	2K	2.5K	16K	20K
0x0A	1024	1K	1.25K	8K	10K

A write access to this register causes a Software Clear. This register must not be written while acquisition is running.

2.16. Buffer Free (0x8010; r/w)

Bit	Function
[11:0]	N = Frees the first N Output Buffer Memory Blocks

2.17. Custom Size (0x8020; r/w)

Bit	Function
[31:0]	0= Custom Size disabled N_{LOC} (≠0) = Number of memory locations per event (1 location = 2 samples or 2 locations = 5 samples when Pack2.5 mode is used)

This register must not be written while acquisition is running.

2.18. Acquisition Control (0x8100; r/w)

Bit	Function
[3]	0 = COUNT ACCEPTED TRIGGERS 1 = COUNT ALL TRIGGERS allows to reject overlapping triggers
[2]	0 = Acquisition STOP 1 = Acquisition RUN allows to RUN/STOP Acquisition
[1:0]	00 = REGISTER-CONTROLLED RUN MODE 01 = S-IN CONTROLLED RUN MODE 10 = S-IN GATE MODE 11 = MULTI-BOARD SYNC MODE

Bit [2] allows to Run and Stop data acquisition; when such bit is set to 1 the board enters Run mode and a Memory Reset) is automatically performed. When bit [2] is reset to 0 the stored data are kept available for readout. In Stop Mode all triggers are neglected.
Bits [1:0] descritpion:
00 = REGISTER-CONTROLLED RUN MODE: multiboard synchronisation via S_IN front panel signal

- RUN control: start/stop via set/clear of bit[2]
- GATE always active (Continuous Gate Mode)

01 = S-IN CONTROLLED RUN MODE: Multiboard synchronisation via S-IN front panel signal

- S-IN works both as SYNC and RUN_START command
- GATE always active (Continuous Gate Mode)

10 = S-IN GATE MODE

- Multiboard synchronisation is disabled
- S-IN works as Gate signal set/clear of RUN/STOP bit

11 = MULTI-BOARD SYNC MODE

- Used only for Multiboard synchronisation

2.19. Acquisition Status (0x8104; r)

Bit	Function
[8]	Board ready for acquisition (PLL and ADCs are synchronised correctly) 0 = not ready 1 = ready This bit should be checked after software reset to ensure that the board will enter immediatly run mode after RUN mode setting; otherwise a latency between RUN mode setting and Acquisition start might occur.
[7]	PLL Status Flag: 0 = PLL loss of lock 1 = no PLL loss of lock NOTE: flag can be restored to 1 via read access to Status Register (see § 2.34)
[6]	PLL Bypass mode: 0 = No bypass mode 1 = Bypass mode
[5]	Clock source: 0 = Internal 1 = External
[4]	EVENT FULL: it is set to 1 as the maximum nr. of events to be read is reached
[3]	EVENT READY: it is set to 1 as at least one event is available to readout
[2]	0 = RUN off 1 = RUN on
[1:0]	*reserved*

2.20. Software Trigger (0x8108; w)

Bit	Function
[31:0]	A write access to this location generates a trigger via software

2.21. Trigger Source Enable Mask (0x810C; r/w)

Bit	Function
[31]	0 = Software Trigger Disabled 1 = Software Trigger Enabled
[30]	0 = External Trigger Disabled 1 = External Trigger Enabled
[29:27]	*reserved*
[26:24]	Local trigger coincidence level (default = 0)
[23:8]	*reserved*
[7]	0 = Channel 7 trigger disabled 1 = Channel 7 trigger enabled
[6]	0 = Channel 6 trigger disabled 1 = Channel 6 trigger enabled
[5]	0 = Channel 5 trigger disabled 1 = Channel 5 trigger enabled
[4]	0 = Channel 4 trigger disabled 1 = Channel 4 trigger enabled
[3]	0 = Channel 3 trigger disabled 1 = Channel 3 trigger enabled
[2]	0 = Channel 2 trigger disabled 1 = Channel 2 trigger enabled
[1]	0 = Channel 1 trigger disabled 1 = Channel 1 trigger enabled
[0]	0 = Channel 0 trigger disabled 1 = Channel 0 trigger enabled

This register bits[0,7] enable the channels to generate a local trigger as the digitised signal exceeds the Vth threshold. Bit0 enables Ch0 to generate the trigger, bit1 enables Ch1 to generate the trigger and so on.
Bits [26:24] allows to set minimum number of channels that must be over threshold, beyond the triggering channel, in order to actually generate the local trigger signal; for example if bit[7:0]=FF (all channels enabled) and Local trigger coincidence level = 1, whenever one channel exceeds the threshold, the trigger will be generated only if at least another channel is over threshold at that moment. Local trigger coincidence level must be smaller than the number of channels enabled via bit[7:0] mask.
EXTERNAL TRIGGER ENABLE (bit30) enables the board to sense TRG-IN signals
SW TRIGGER ENABLE (bit 31) enables the board to sense software trigger (see § 2.20).

2.22. Front Panel Trigger Out Enable Mask (0x8110; r/w)

Bit	Function
[31]	0 = Software Trigger Disabled 1 = Software Trigger Enabled
[30]	0 = External Trigger Disabled 1 = External Trigger Enabled
[29:8]	*reserved*
[7]	0 = Channel 7 trigger disabled 1 = Channel 7 trigger enabled
[6]	0 = Channel 6 trigger disabled 1 = Channel 6 trigger enabled
[5]	0 = Channel 5 trigger disabled 1 = Channel 5 trigger enabled
[4]	0 = Channel 4 trigger disabled 1 = Channel 4 trigger enabled
[3]	0 = Channel 3 trigger disabled 1 = Channel 3 trigger enabled
[2]	0 = Channel 2 trigger disabled 1 = Channel 2 trigger enabled
[1]	0 = Channel 1 trigger disabled 1 = Channel 1 trigger enabled
[0]	0 = Channel 0 trigger disabled 1 = Channel 0 trigger enabled

This register bits[0,7] enable the channels to generate a TRG_OUT front panel signal as the digitised signal exceeds the Vth threshold.
Bit0 enables Ch0 to generate the TRG_OUT, bit1 enables Ch1 to generate the TRG_OUT and so on.
EXTERNAL TRIGGER ENABLE (bit30) enables the board to generate the TRG_OUT
SW TRIGGER ENABLE (bit 31) enables the board to generate TRG_OUT (see § 2.20).

2.23. Post Trigger Setting (0x8114; r/w)

Bit	Function
[31:0]	Post trigger value

Allows to set the number of post trigger samples:
Npost = PostTriggerValue*4 + ConstantLatency; where:
Npost = number of post trigger samples.
PostTriggerValue = Content of this register.
ConstantLatency = constant number of samples added due to the latency associated to the trigger processing logic in the ROC FPGA; this value is constant, but the exact value may change between different firmware revisions.

2.24. Front Panel I/O Data (0x8118; r/w)

Bit	Function
[15:0]	Front Panel I/O Data

Allows to Readout the logic level of LVDS I/Os and set the logic level of LVDS Outputs.

2.25. Front Panel I/O Control (0x811C; r/w)

Bit	Function
[15]	0 = I/O Normal operations: TRG-OUT signals outside trigger presence (trigger are generated according to Front Panel Trigger Out Enable Mask setting, see § 2.22) 1= I/O Test Mode: TRG-OUT is a logic level set via bit 14
[14]	1= TRG-OUT Test Mode set to 1 0 = TRG-OUT Test Mode set to 0
[13:10]	*reserved*
[9]	PATTERN_LATCH_MODE 0 = PATTERN field into event headers is the status of 16 LVDS Front Panel Inputs latched with board internal trigger (if a post trigger value is set, the internal trigger is delayed respect to external one). 1 = PATTERN field into event headers is the status of 16 LVDS Front Panel Inputs latched with external trigger rising edge.
[8]	*reserved*
[7:6]	00 = General Purpose I/O 01 = Programmed I/O 10 = Pattern mode: LVDS signals are input and their value is written into header PATTERN field
[5]	0 = LVDS I/O 15..12 are inputs 1 = LVDS I/O 15..12 are outputs
[4]	0 = LVDS I/O 11..8 are inputs 1 = LVDS I/O 11..8 are outputs
[3]	0 = LVDS I/O 7..4 are inputs 1 = LVDS I/O 7..4 are outputs
[2]	0 = LVDS I/O 3..0 are inputs 1 = LVDS I/O 3..0 are outputs
[1]	0= panel output signals (TRG-OUT/CLKOUT) enabled 1= panel output signals (TRG-OUT/CLKOUT) enabled in high impedance
[0]	0 = TRG/CLK are NIM I/O Levels 1 = TRG/CLK are TTL I/O Levels

Bits [5:2] are meaningful for General Purpose I/O use only

2.26. Channel Enable Mask (0x8120; r/w)

Bit	Function
[7]	0 = Channel 7 disabled 1 = Channel 7 enabled
[6]	0 = Channel 6 disabled 1 = Channel 6 enabled
[5]	0 = Channel 5 disabled 1 = Channel 5 enabled
[4]	0 = Channel 4 disabled 1 = Channel 4 enabled
[3]	0 = Channel 3 disabled 1 = Channel 3 enabled
[2]	0 = Channel 2 disabled 1 = Channel 2 enabled
[1]	0 = Channel 1 disabled 1 = Channel 1 enabled
[0]	0 = Channel 0 disabled 1 = Channel 0 enabled

Enabled channels provide the samples which are stored into the events (and not erased). The mask cannot be changed while acquisition is running.

2.27. ROC FPGA Firmware Revision (0x8124; r)

Bit	Function
[31:16]	Revision date in Y/M/DD format
[15:8]	Firmware Revision (X)
[7:0]	Firmware Revision (Y)

Bits [31:16] contain the Revision date in Y/M/DD format.
Bits [15:0] contain the firmware revision number coded on 16 bit (X.Y format).

2.28. Event Stored (0x812C; r)

Bit	Function
[31:0]	This register contains the number of events currently stored in the Output Buffer

This register value cannot exceed the maximum number of available buffers according to setting of buffer size register.

2.29. Set Monitor DAC (0x8138; r/w)

Bit	Function
[11:0]	This register allows to set the DAC value (12bit)

This register allows to set the DAC value in Voltage level mode.
LSB = 0.244 mV, terminated on 50 Ohm.

2.30. Board Info (0x8140; r)

Bit	Function
[15:8]	Memory size (Mbyte/channel)
[7:0]	Board Type: 0x03 = V1720

2.31. Monitor Mode (0x8144; r/w)

Bit	Function
[2:0]	This register allows to encode the Analog Monitor operation: 000 = majority 001 = waveform generator (saw tooth ramp) 010 = *reserved* 011 = buffer occupancy 100 = voltage level

2.32. Event Size (0x814C; r)

Bit	Function
[31:0]	Nr. of 32 bit words in the next event

2.33. VME Control (0xEF00; r/w)

Bit	Function
[7]	0 = Release On Register Access (RORA) Interrupt mode (default) 1 = Release On AcKnowledge (ROAK) Interrupt mode
[6]	0 = RELOC Disabled (BA is selected via Rotary Switch 1 = RELOC Enabled (BA is selected via RELOC register; see § 2.37)
[5]	0 = ALIGN64 Disabled 1 = ALIGN64 Enabled
[4]	0 = BERR Not Enabled; the module sends a DTACK signal until the CPU inquires the module 1 = BERR Enabled; the module is enabled either to generate a Bus error to finish a block transfer or during the empty buffer read out in D32
[3]	0 = Optical Link interrupt disabled 1 = Optical Link interrupt enabled
[2 :0]	Interrupt level (0= interrupt disabled)

Bit [7]: this setting is valid only for interrupts broadcasted on VMEbus; interrupts broadcasted on optical link feature RORA mode only.

- In RORA mode, interrupt status can be removed by accessing VME Control register (see § 2.33) and disabling the active interrupt level.
- In ROAK mode, interrupt status is automatically removed via an interrupt acknowledge cycle.

Interrupt generation is restored by setting an Interrupt level > 0 via VME Control register.

2.34. VME Status (0xEF04; r)

Bit	Function
[2]	0 = BERR FLAG: no Bus Error has occurred 1 = BERR FLAG: a Bus Error has occurred (this bit is re-set after a status register read out)
[1]	0 = The Output Buffer is not FULL; 1 = The Output Buffer is FULL.
[0]	0 = No Data Ready; 1 = Event Ready

2.35. Board ID (0xEF08; r/w)

Bit	Function
[4 :0]	GEO

- VME64X versions: this register can be accessed in read mode only and contains the GEO address of the module picked from the backplane connectors; when CBLT is performed, the GEO address will be contained in the EVENT HEADER Board ID field.
- Other versions: this register can be accessed both in read and write mode; it allows to write the correct GEO address (default setting = 0) of the module before CBLT operation. GEO address will be contained in the EVENT HEADER Board ID field)

2.36. MCST Base Address and Control (0xEF0C; r/w)

Bit	Function
[9:8]	Allows to set up the board for daisy chaining: 00 = disabled board 01 = last board 10 = first board 11 = intermediate
[7:0]	These bits contain the most significant bits of the MCST/CBLT address of the module set via VME, i.e. the address used in MCST/CBLT operations.

2.37. Relocation Address (0xEF10; r/w)

Bit	Function
[15..0]	These bits contains the A31...A16 bits of the address of the module: it can be set via VME for a relocation of the Base Address of the module.

2.38. Interrupt Status ID (0xEF14; r/w)

Bit	Function
[31..0]	This register contains the STATUS/ID that the module places on the VME data bus during the Interrupt Acknowledge cycle

2.39. Interrupt Event Number (0xEF18; r/w)

Bit	Function
[9:0]	INTERRUPT EVENT NUMBER

If interrupts are enabled, the module generates a request whenever it has stored in memory a Number of events > INTERRUPT EVENT NUMBER

2.40. BLT Event Number (0xEF1C; r/w)

Bit	Function
[7:0]	This register contains the number of complete events which has to be transferred via BLT/CBLT.

2.41. Scratch (0xEF20; r/w)

Bit	Function
[31:0]	Scratch (*to be used to write/read words for VME test purposes*)

2.42. Software Reset (0xEF24; w)

Bit	Function
[31:0]	A write access to this location allows to perform a software reset

2.43. Software Clear (0xEF28; w)

Bit	Function
[31:0]	A write access to this location clears all the memories

2.44. Flash Enable (0xEF2C; r/w)

Bit	Function
[0]	0 = Flash write ENABLED 1 = Flash write DISABLED

This register is handled by the Firmware upgrade tool.

2.45. Flash Data (0xEF30; r/w)

Bit	Function
[7:0]	Data to be serialized towards the SPI On board Flash

This register is handled by the Firmware upgrade tool.

2.46. Configuration Reload (0xEF34; w)

Bit	Function
[31:0]	A write access to this register causes a software reset, a reload of Configuration ROM parameters and a PLL reconfiguration.